

FIG. 1

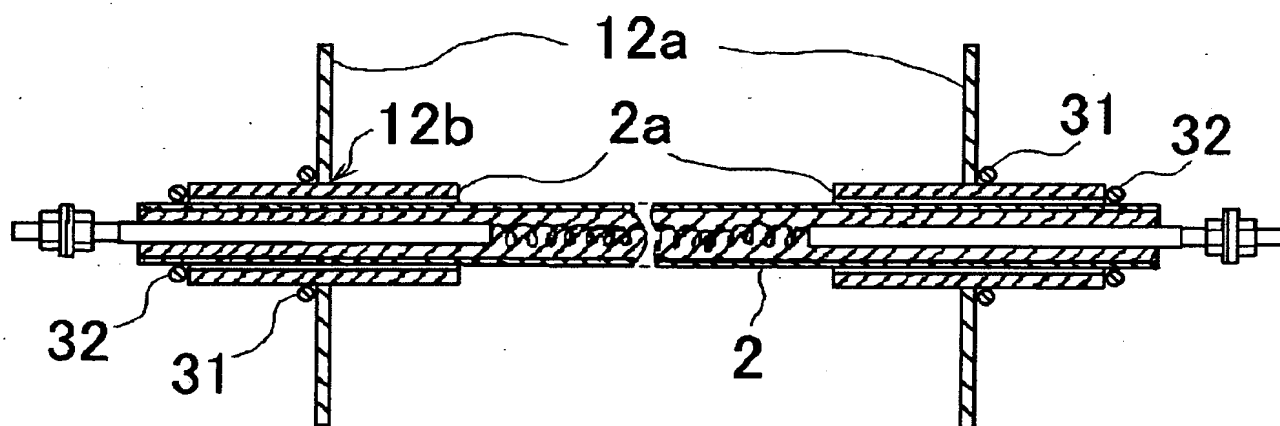


FIG. 2

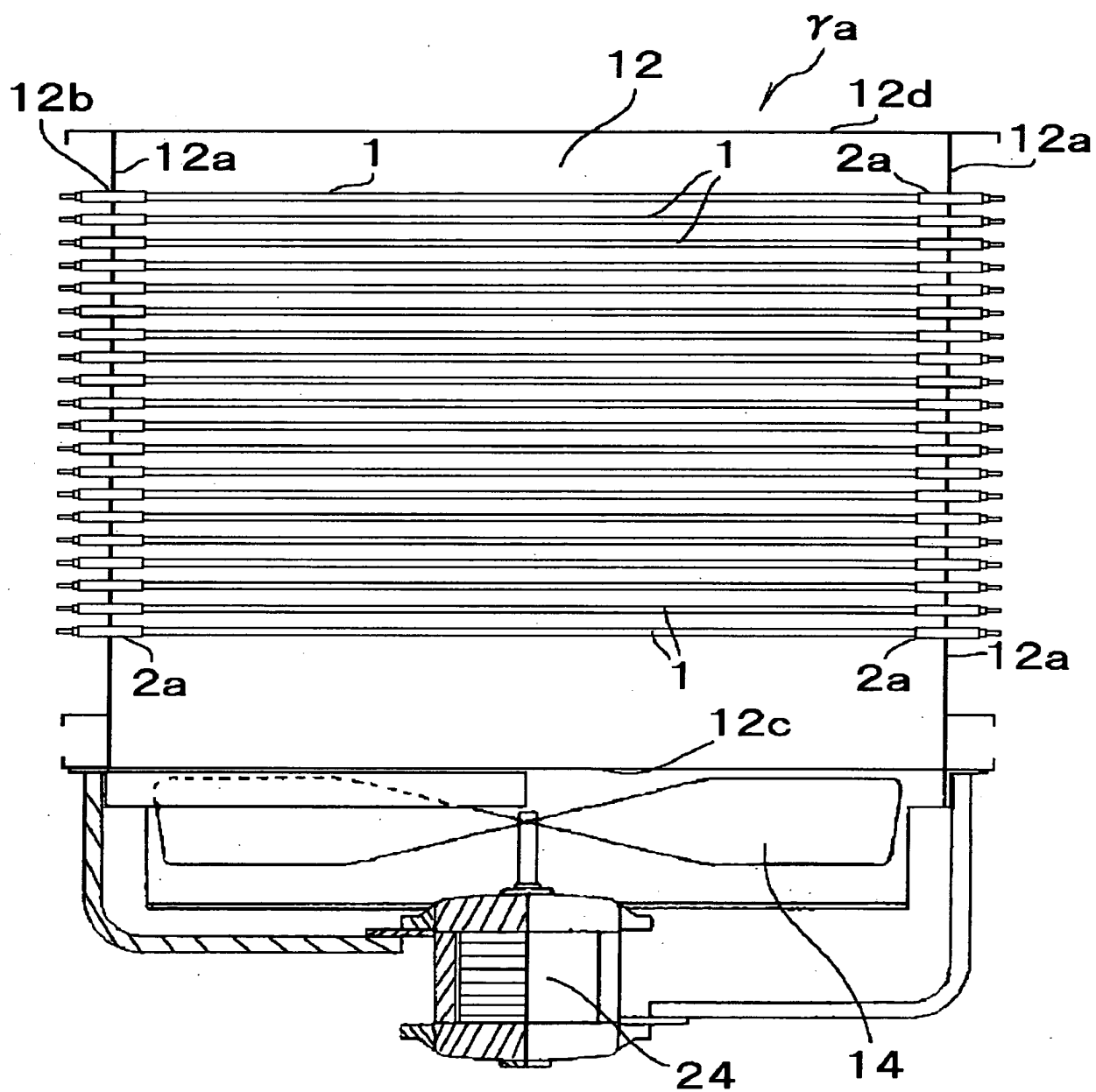


FIG. 3

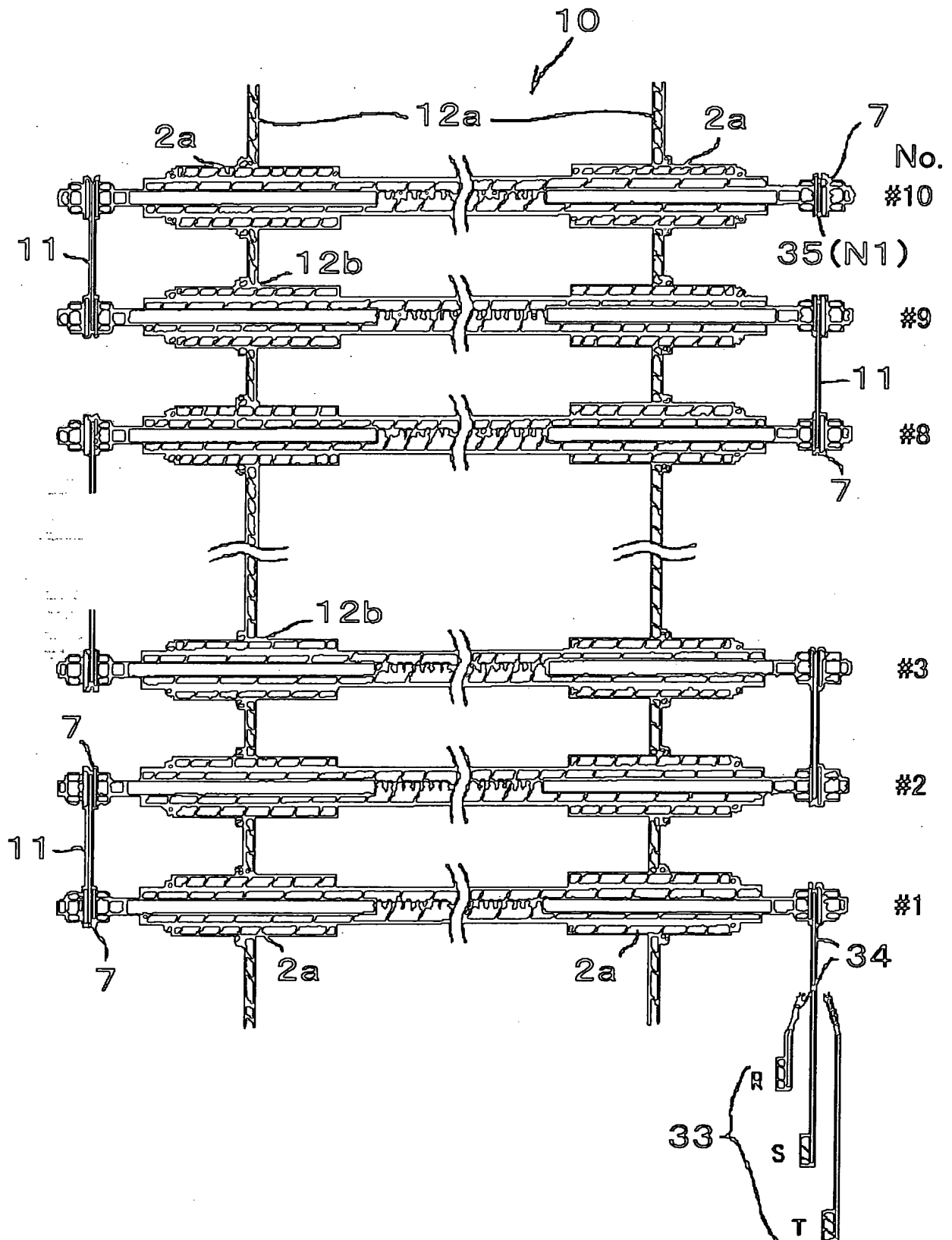


FIG. 4

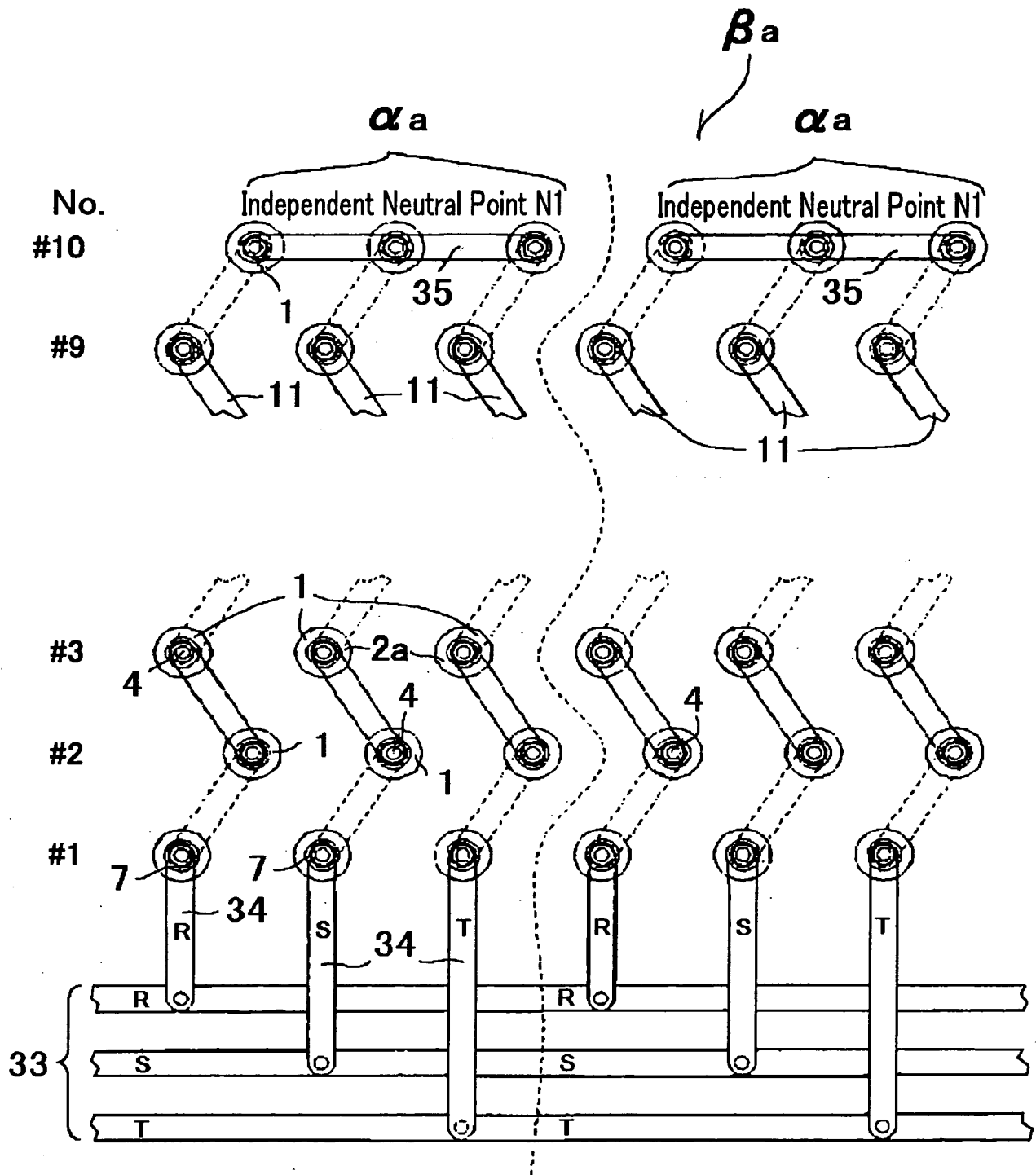


FIG. 5

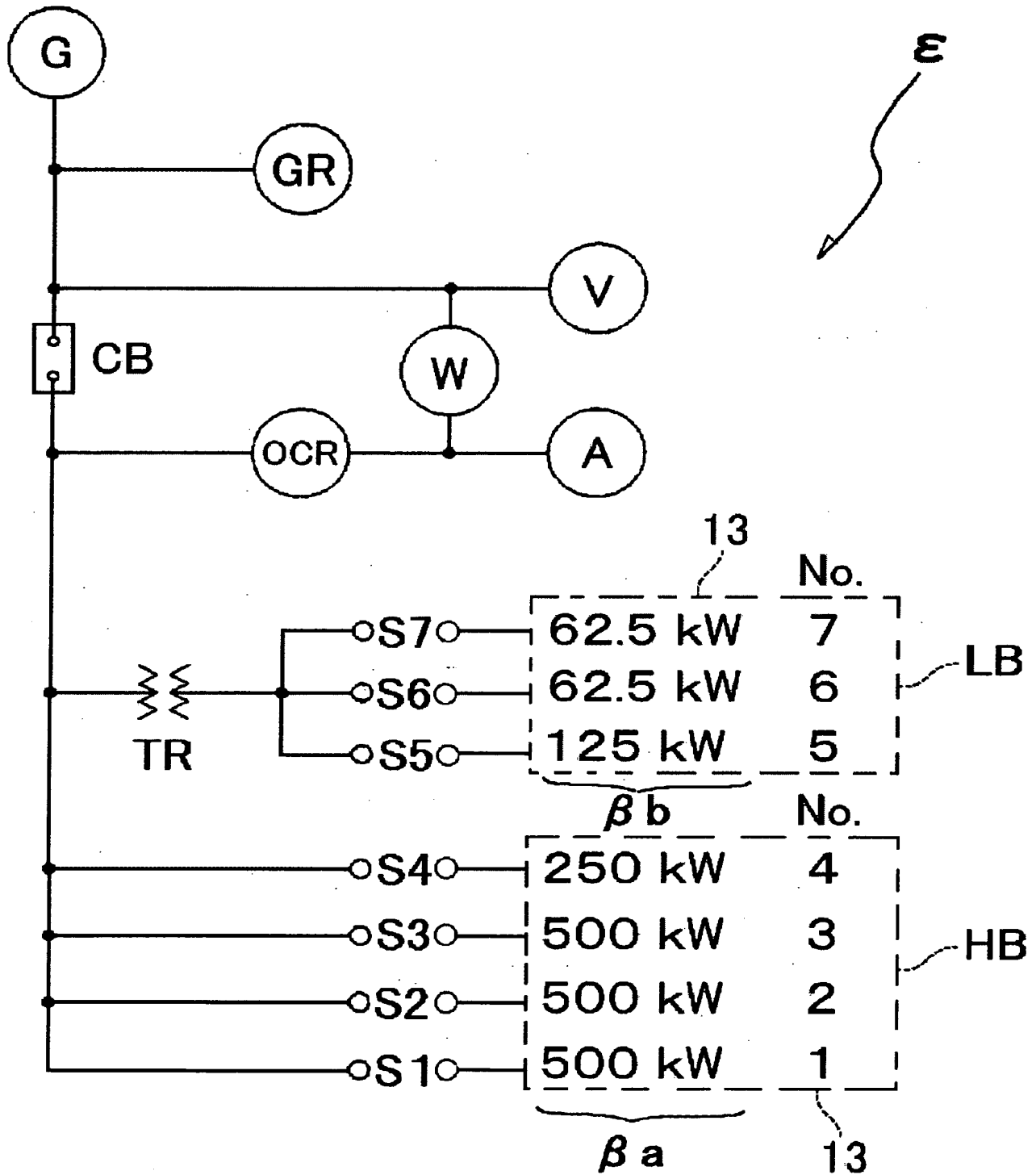


FIG. 6

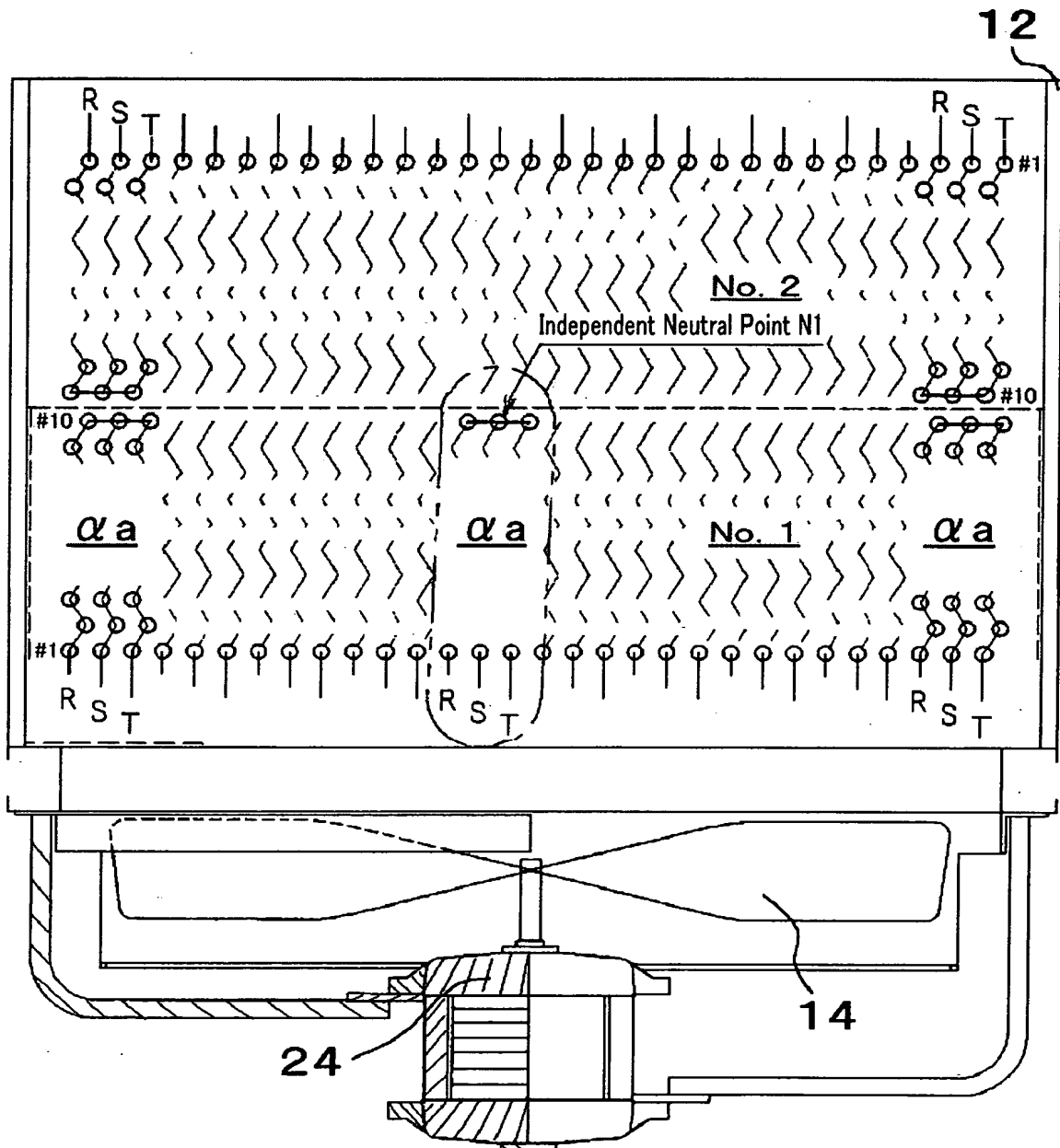


FIG. 7

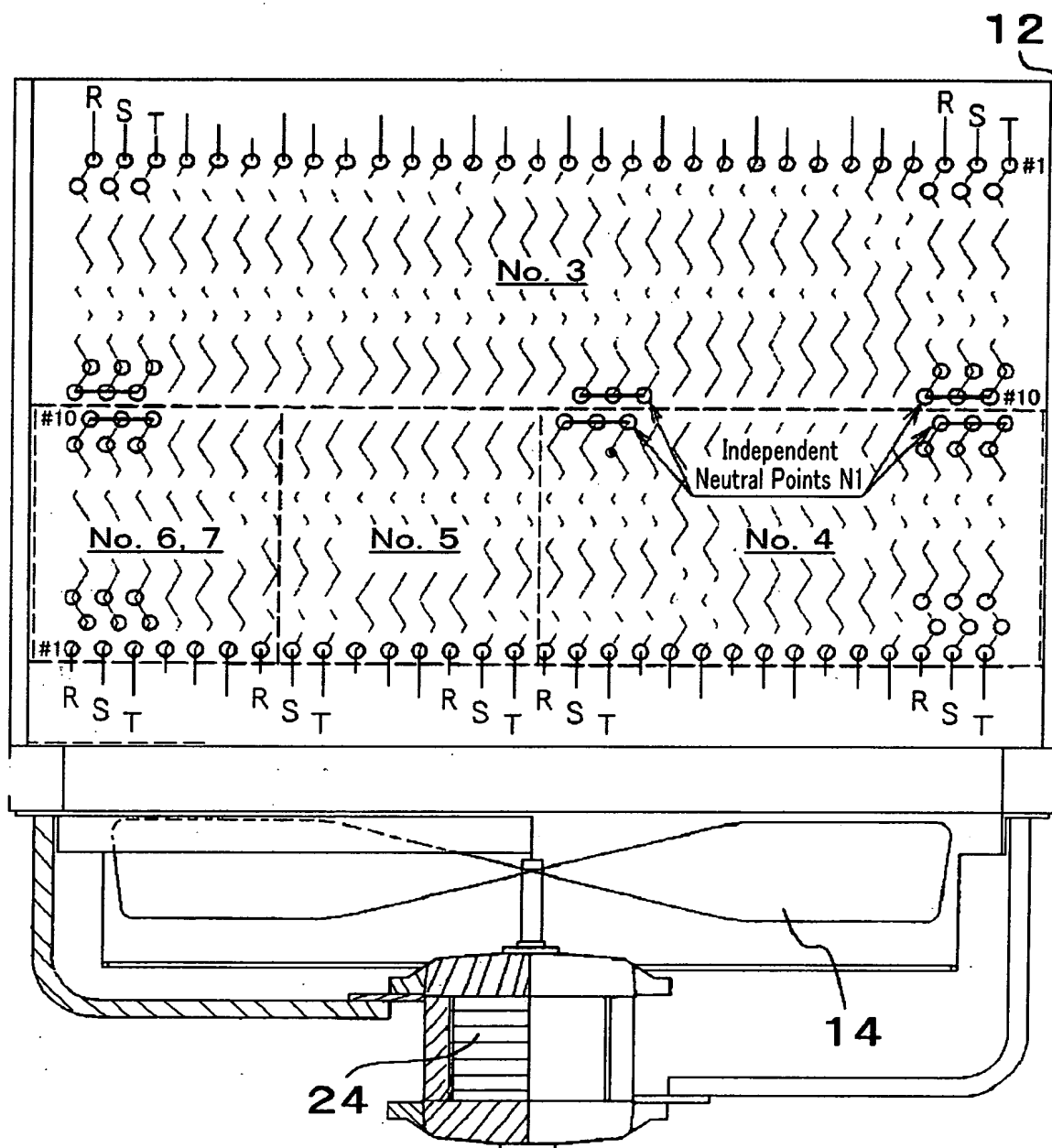


FIG. 8

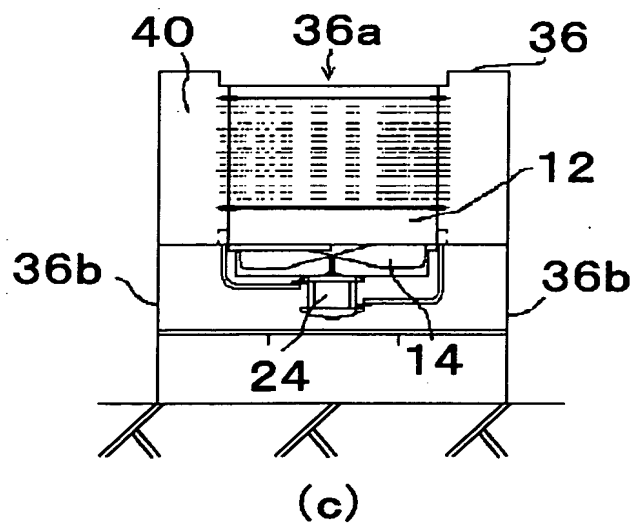
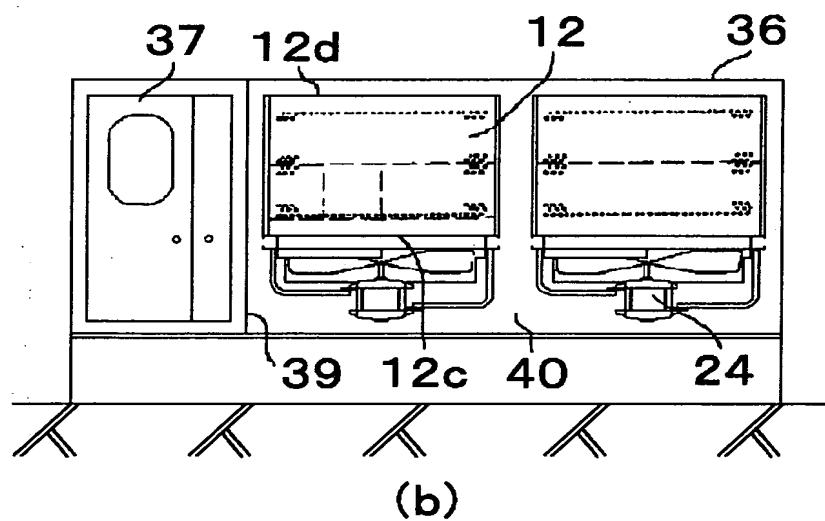
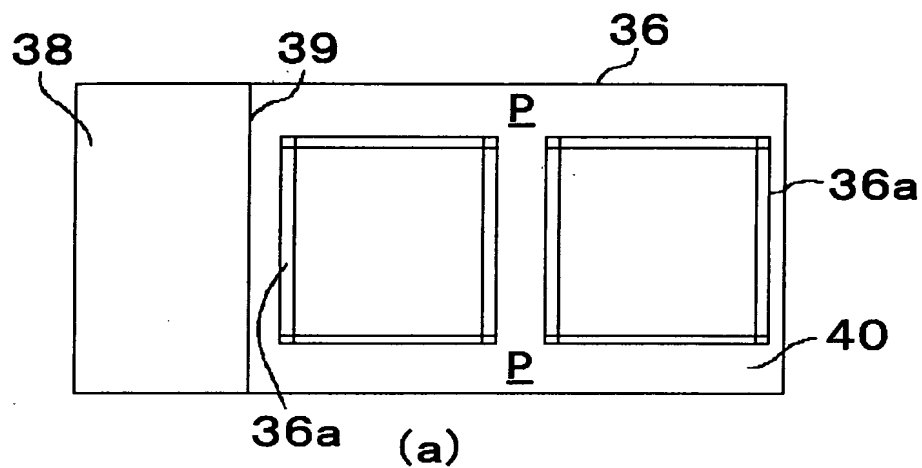
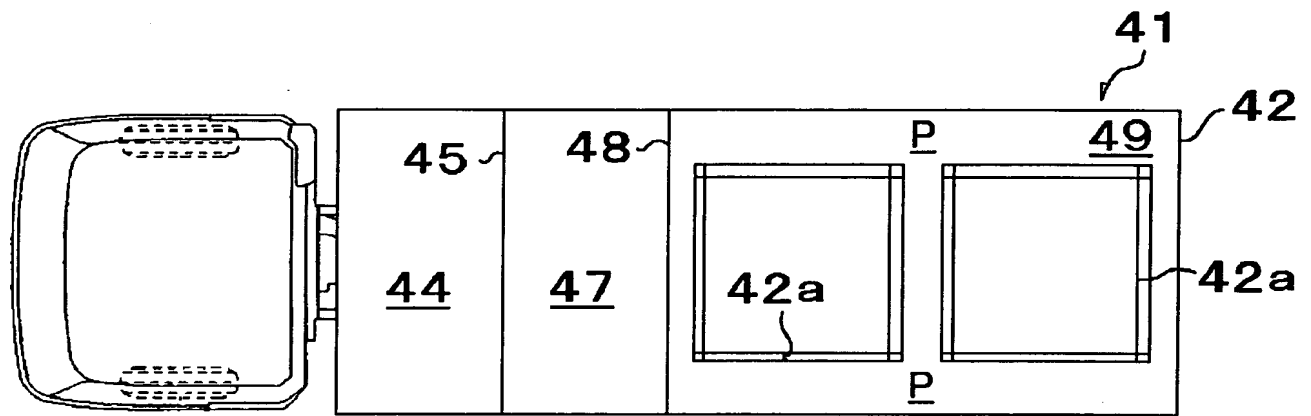
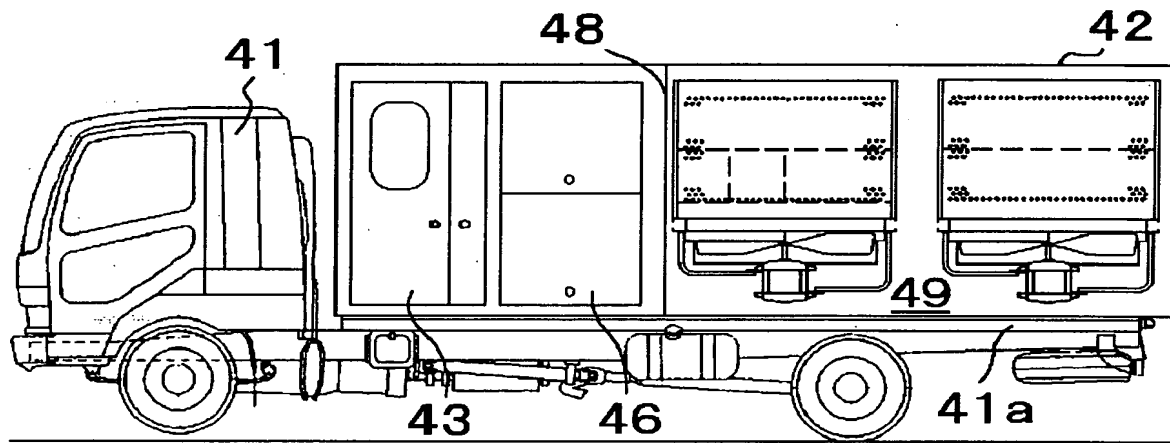


FIG. 9

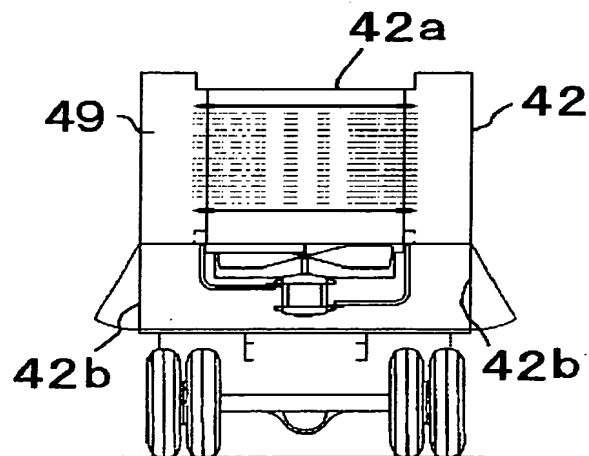
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(a)



(b)



(c)

FIG. 10

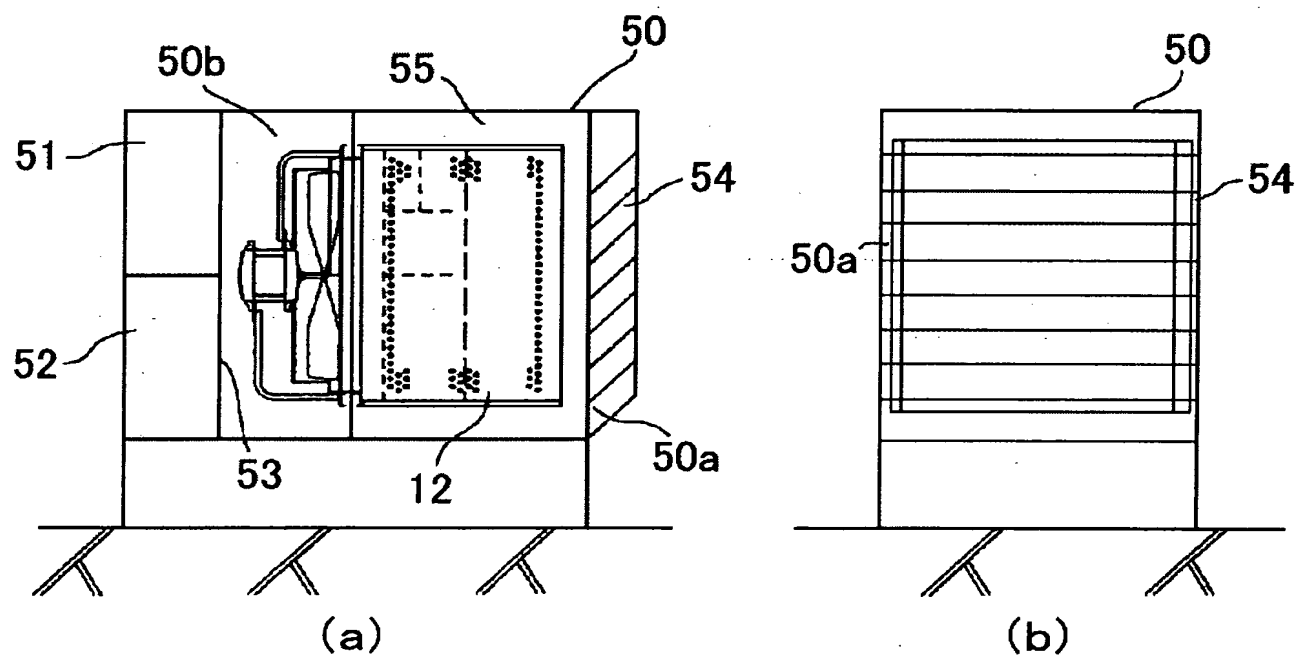


FIG. 11

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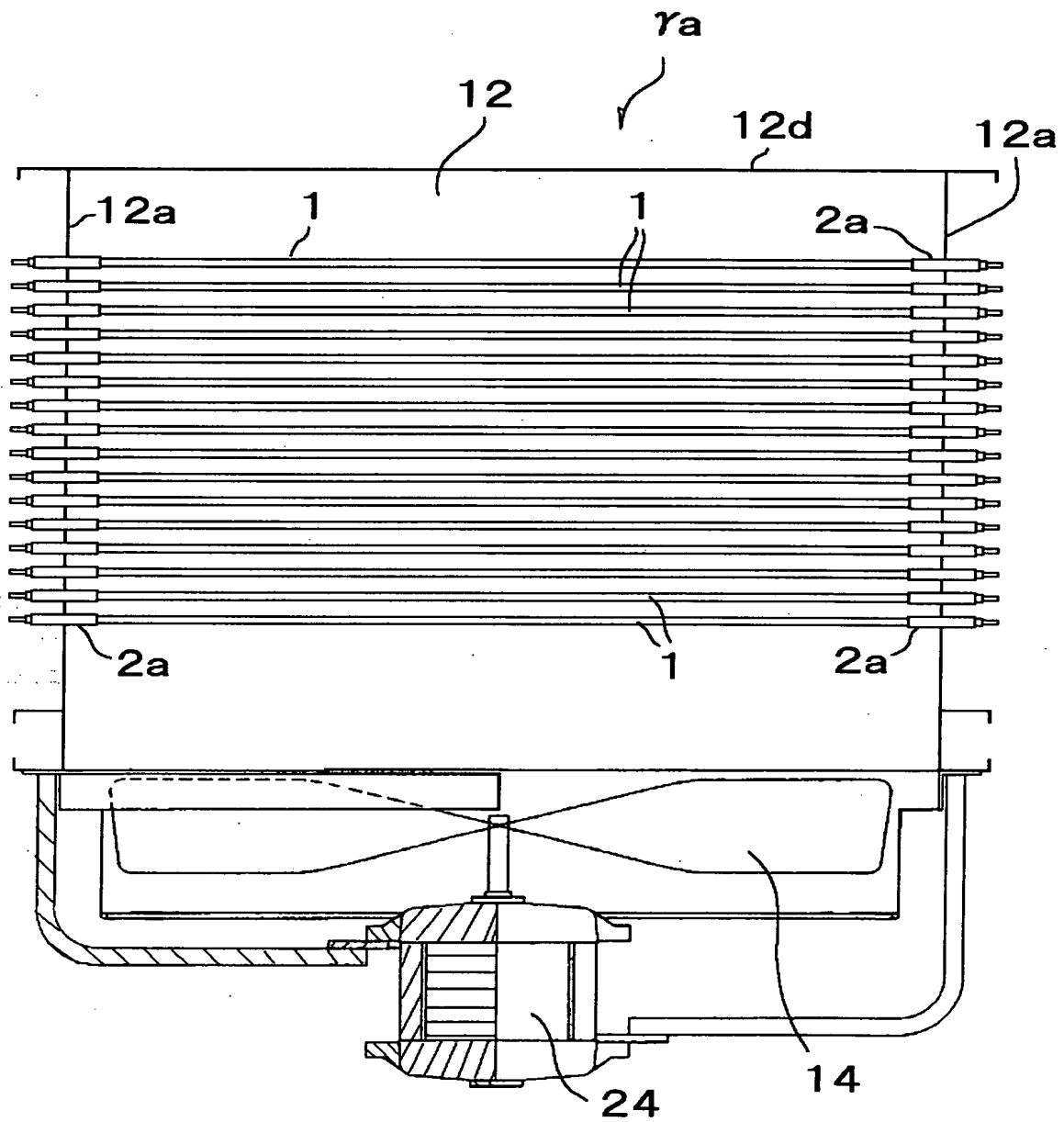


FIG. 12

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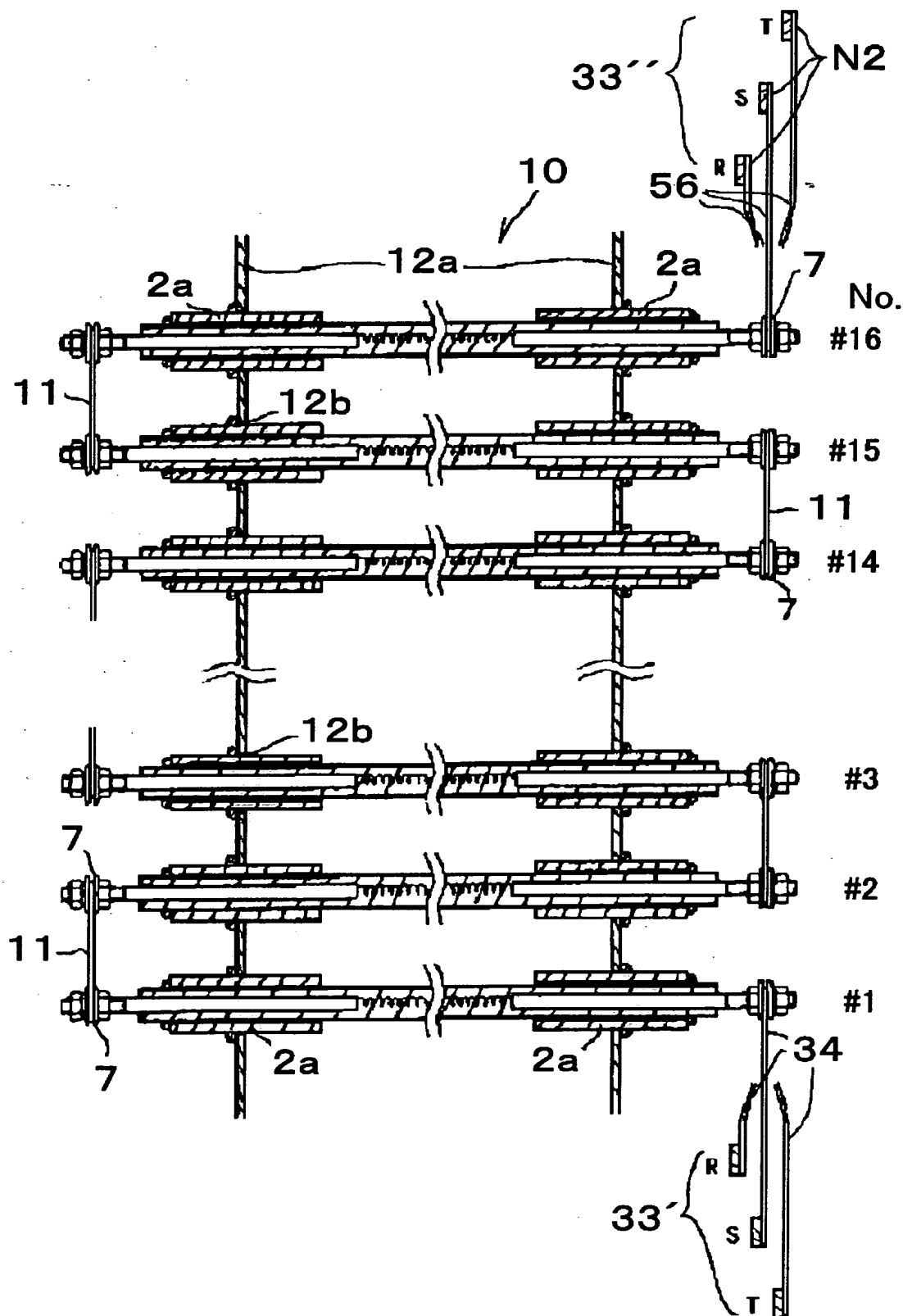


FIG. 13

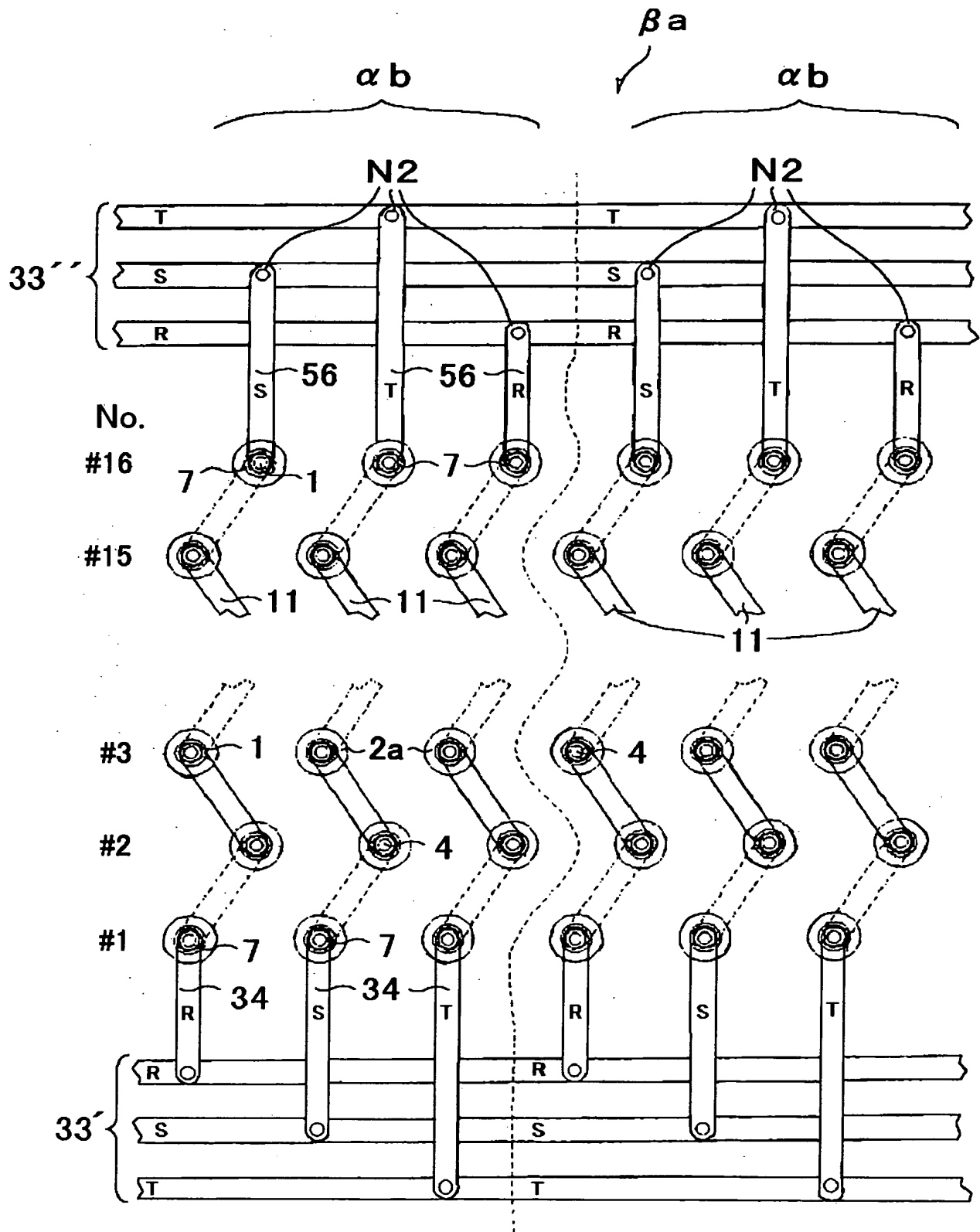


FIG. 14

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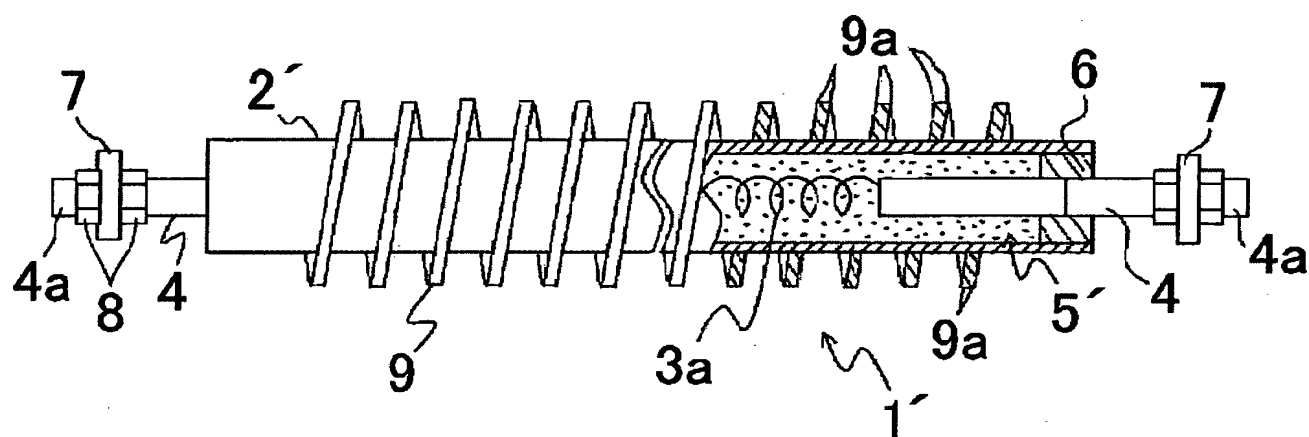


FIG. 15

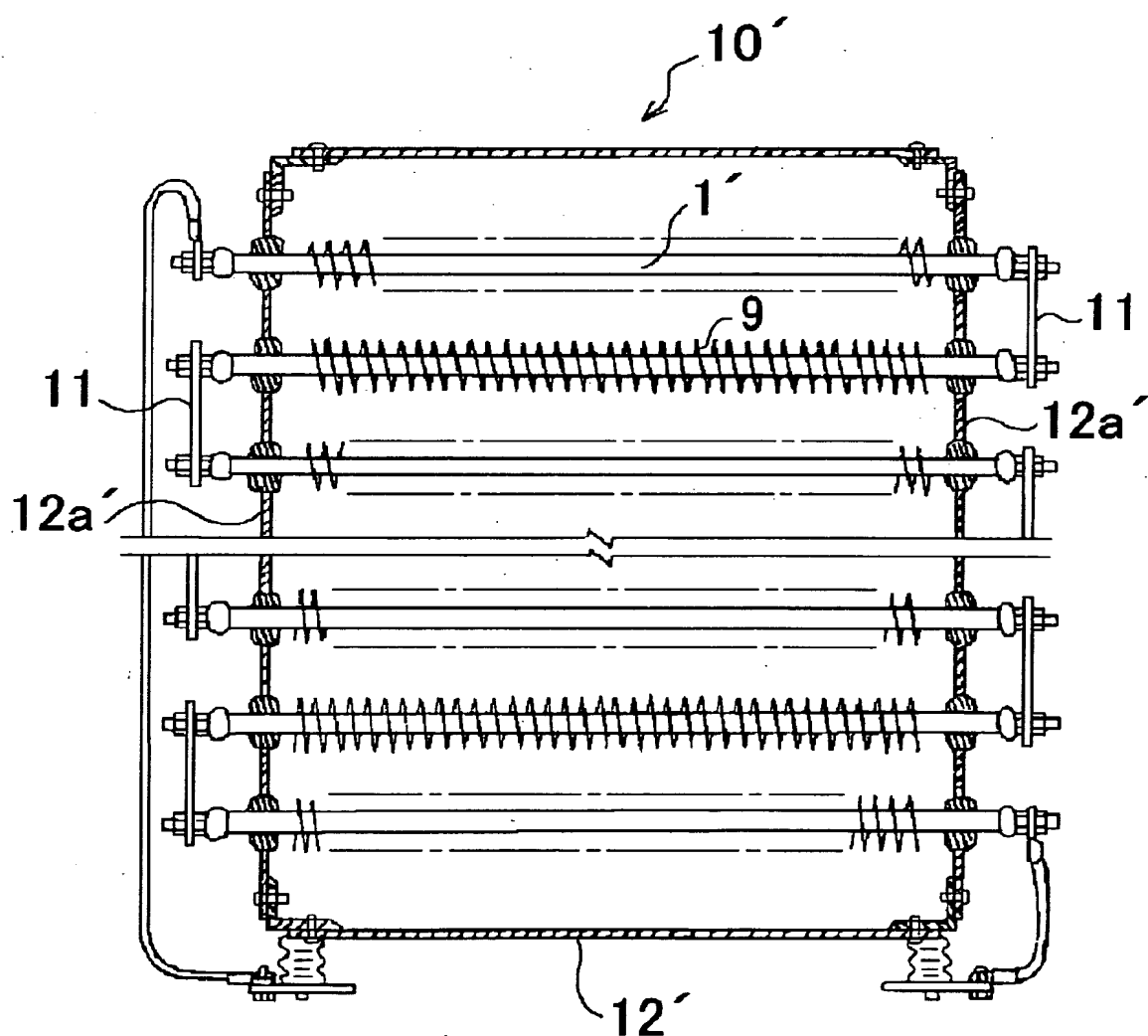


FIG. 16

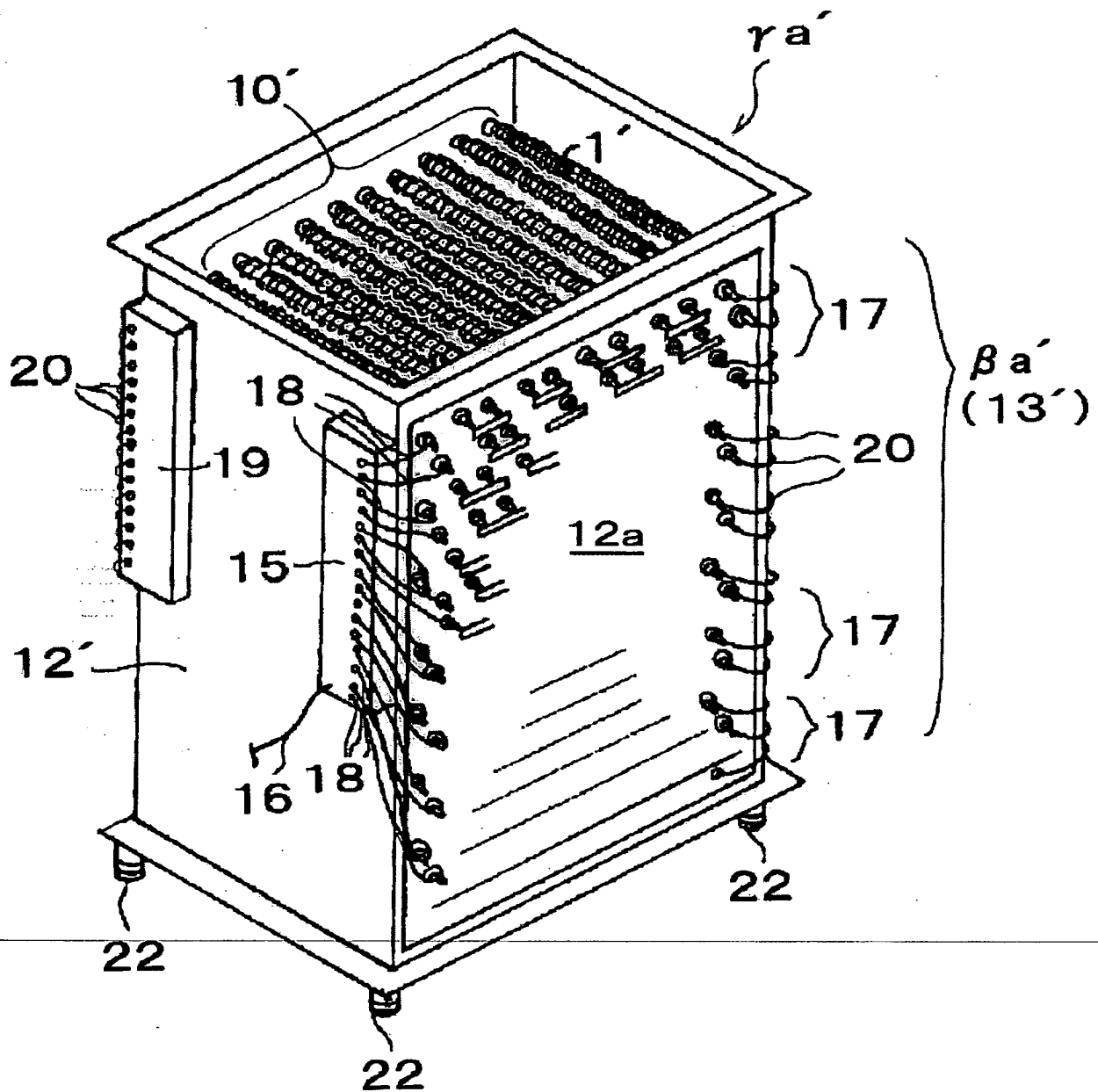


FIG. 17

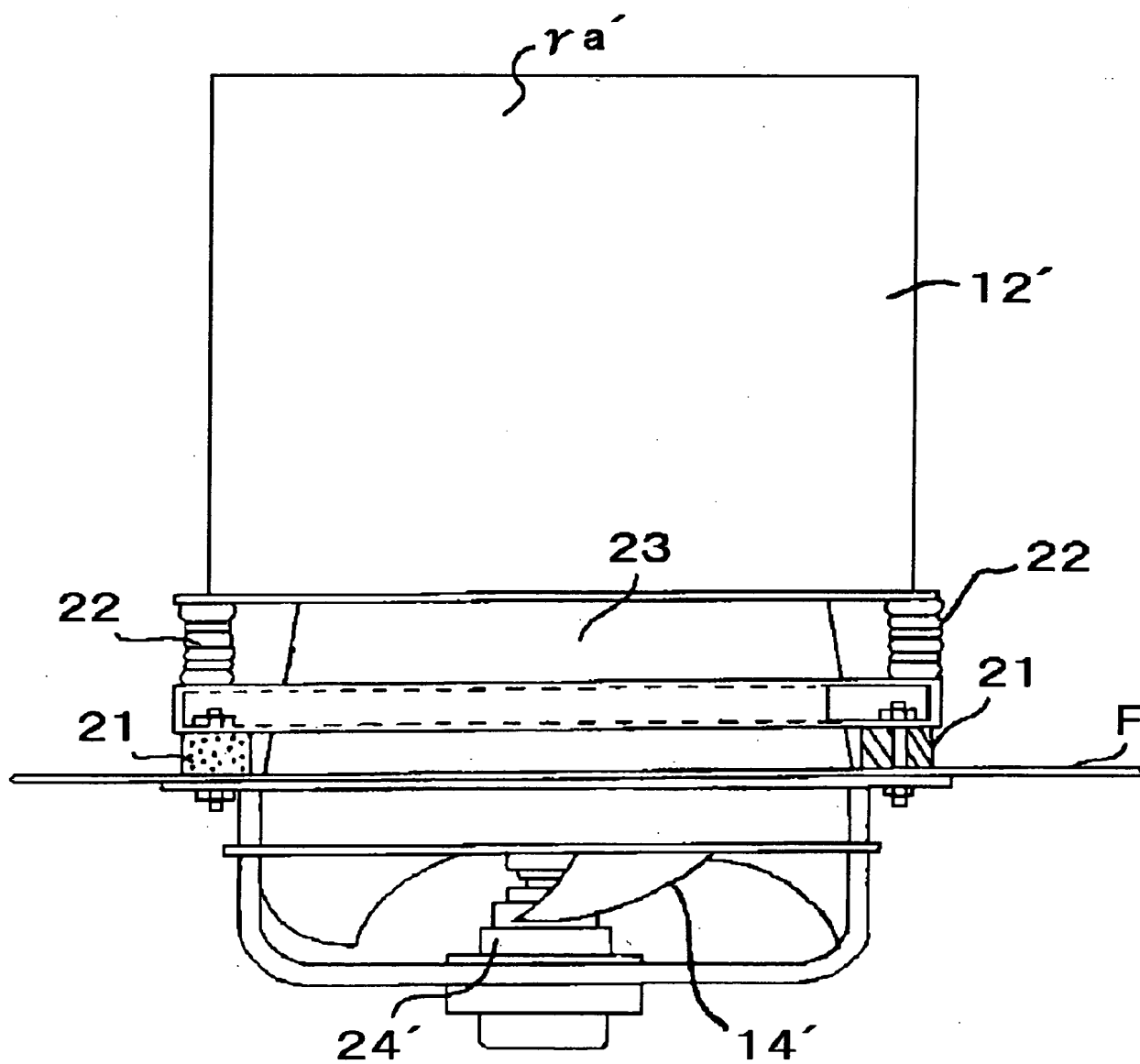


FIG. 18

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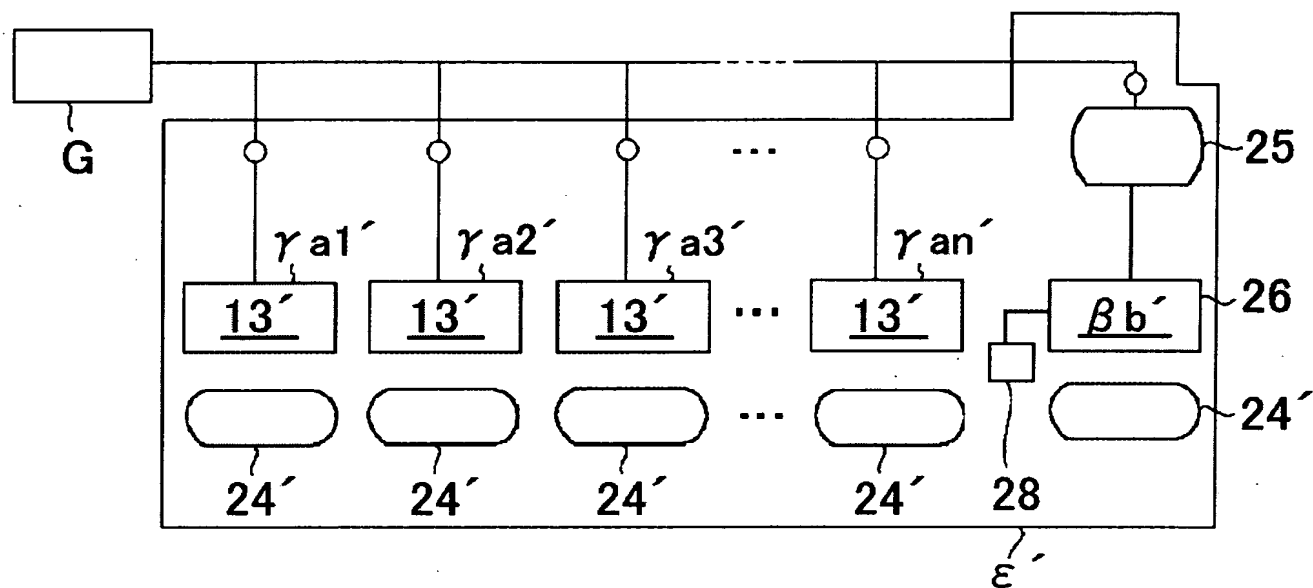
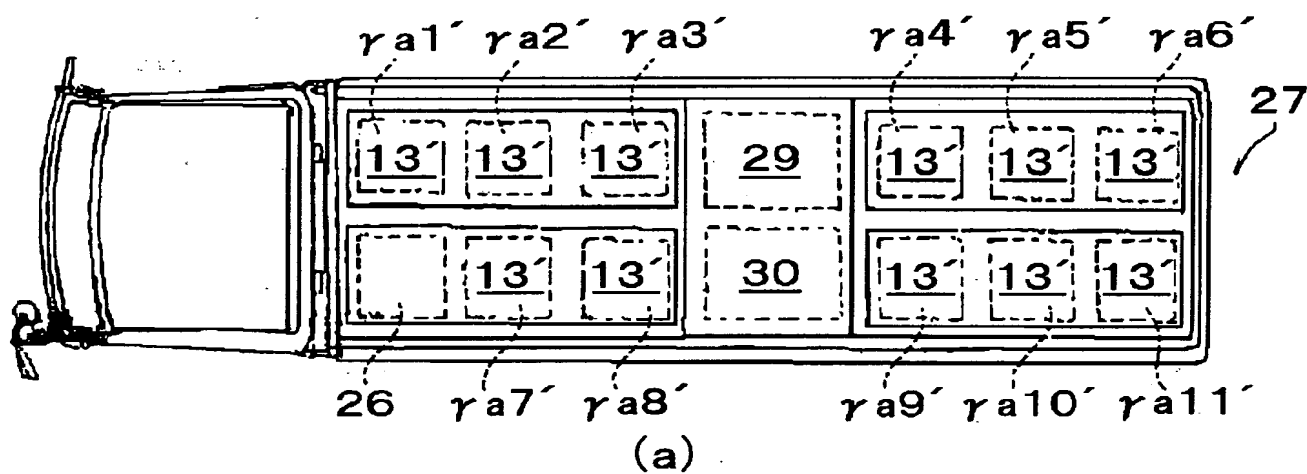
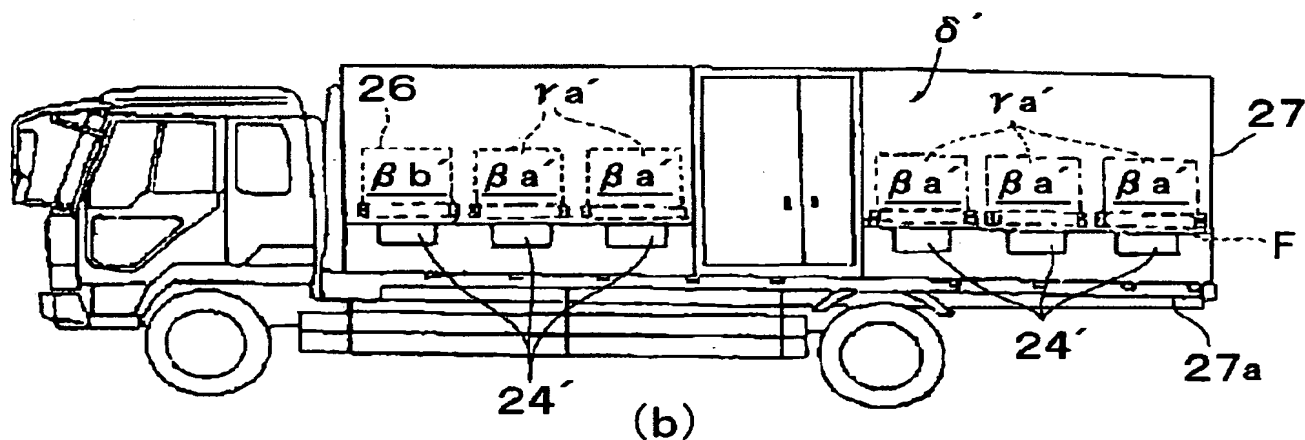


FIG. 19



(a)



(b)

FIG. 20

Equivalent Circuit

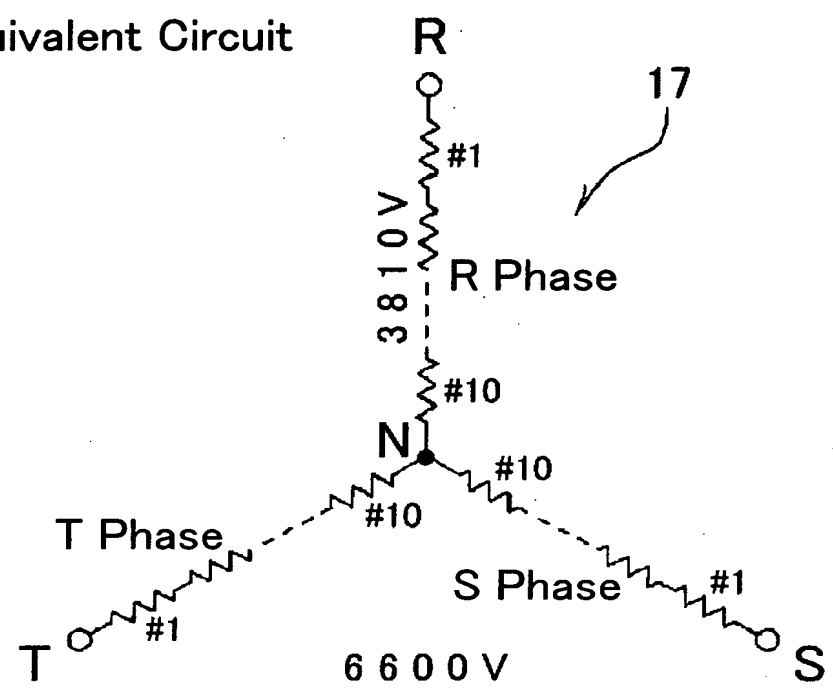


FIG. 21

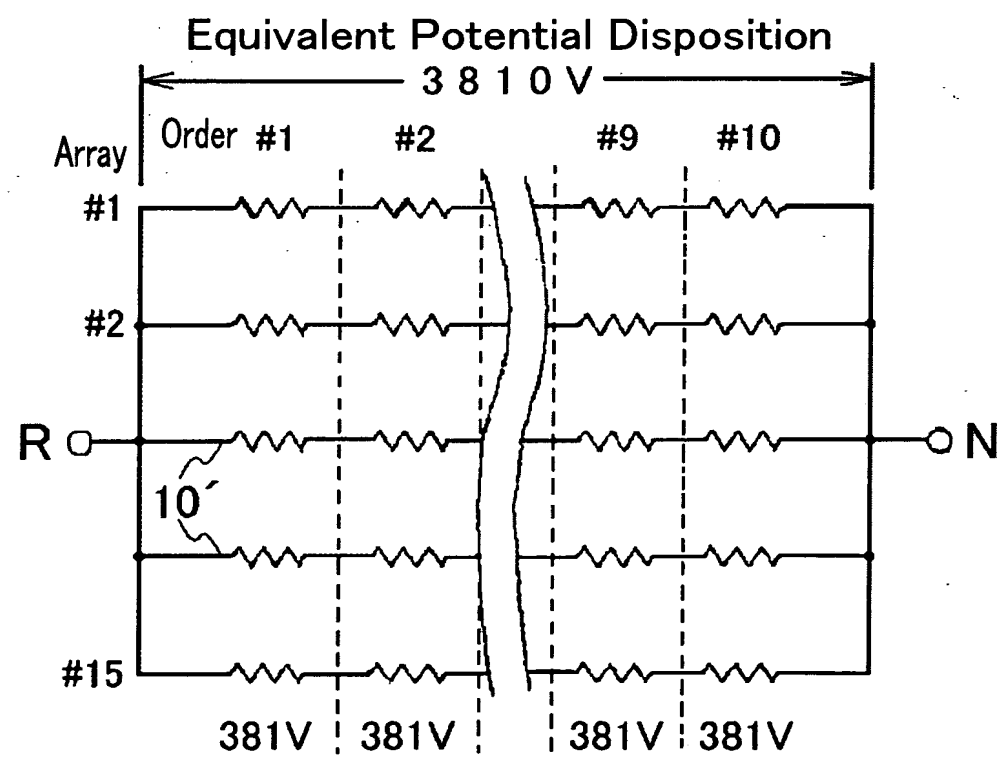


FIG. 22

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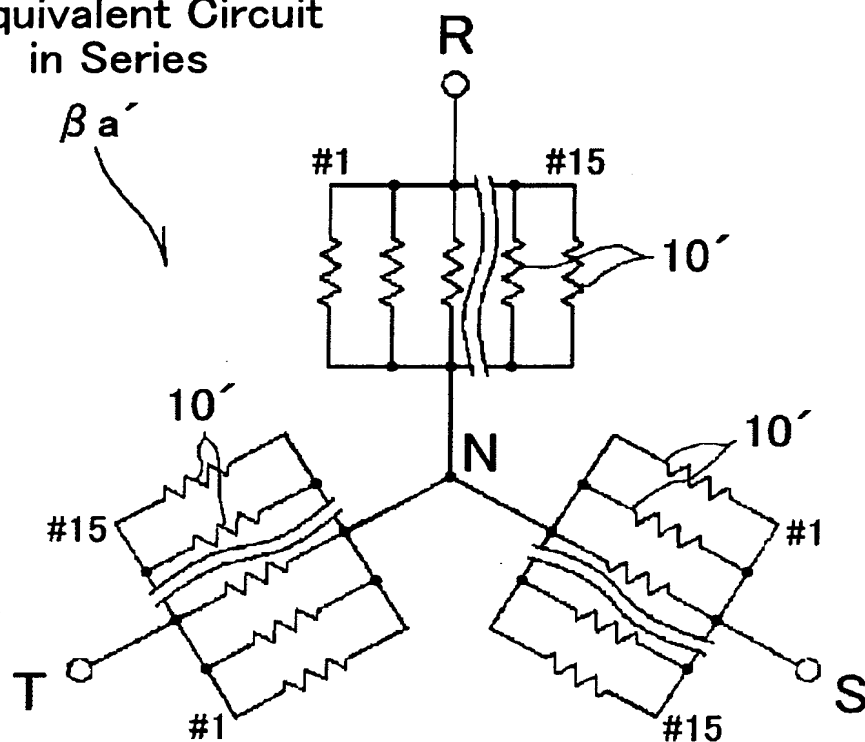
Y Equivalent Circuit
in Series

FIG. 23

R Phase Line One Broken

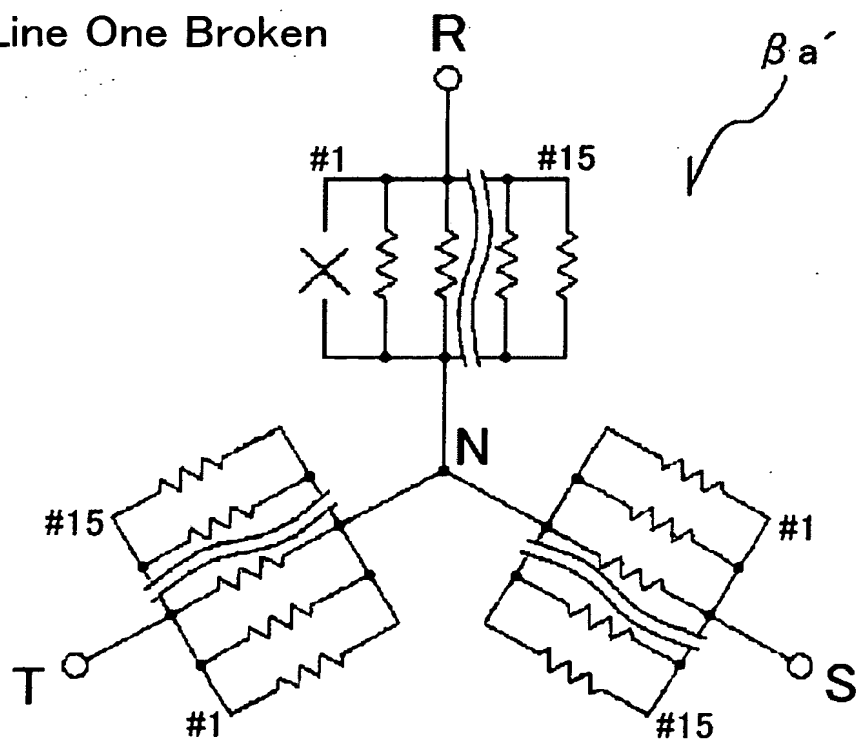
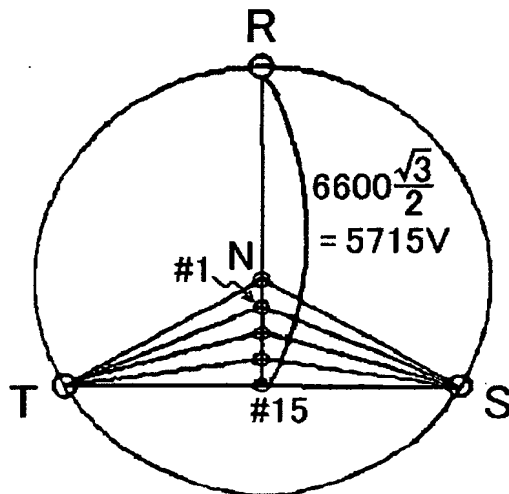


FIG. 24

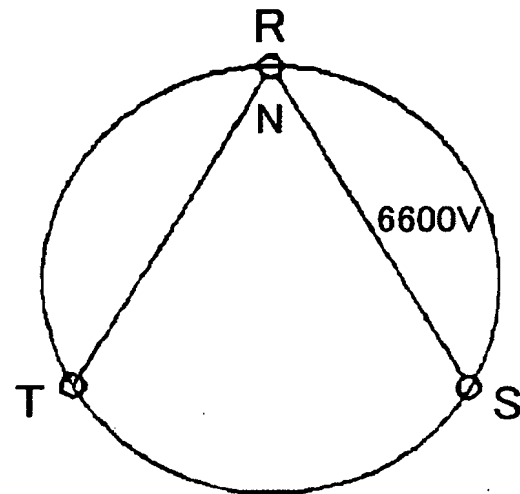
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Potential Rise by Line Broken



(a)

Potential Rise by Short Circuit



(b)

FIG. 25

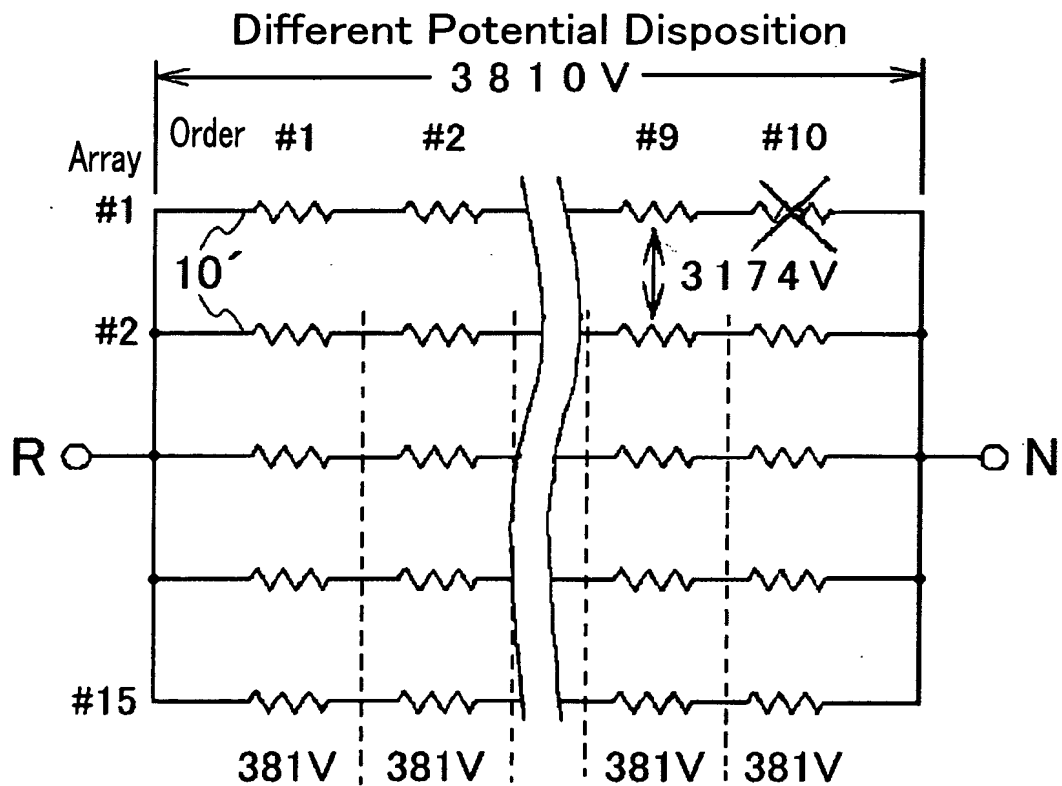


FIG. 26

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